IN THE CLAIMS

Please cancel Claim 8, without prejudice.

Please amend Claims 1, 13, 15 and 22.

LISTING OF THE CLAIMS

1. (currently amended) A method of forming a multi-level semiconductor device wiring interconnect structure according to a low temperature process comprising the steps of:

a) forming a dielectric insulating layer over a conductive portion; said conductive portion comprises silicide electrical contact areas comprising a CMOS transistor portion selected from the group consisting of a gate electrode and source and drain regions;

b) forming a via opening in closed communication with the conductive portion;

c) forming a first barrier layer to line the via opening;

d) then forming a layer of AlCu to fill the via opening to form an AlCu via including a portion of said AlCu layer overlying the dielectric insulating layer; and,

e) forming an AlCu interconnect line from said AlCu portion over the AlCu via, wherein a second barrier layer is optionally formed on said AlCu interconnect line;

wherein process steps c) and d) are carried out at a temperature of less than about 400 degrees Centigrade.

2. (previously presented) The method of claim 1, wherein steps a) through e) are repeated to sequentially form an overlying AlCu via contiguous with an overlying AlCu interconnect line.

3. (previously presented) The method of claim 1, wherein the step of forming a layer of AlCu comprises a magnetron sputtering process carried out at from about room temperature to about 400 °C.

4. (previously presented) The method of claim 3, wherein the magnetron sputtering process is carried out at pressure less than about 5 milliTorr.

5. (original) The method of claim 1, wherein the dielectric insulating layer is selected from the group consisting of carbon doped silicon oxide, organo silicate glass (OSG), and fluorinated silicate glass (FSG).

6. (original) The method of claim 1, wherein the dielectric insulating layer consists essentially of fluorinated silicate glass (FSG).

7. (previously presented) The method of claim 1, wherein the first and second barrier layers is selected from the group consisting of Ti/TiN, TiN, Ta, TaN, and combinations thereof.

8. (cancelled)

9. (original) The method of claim 8, wherein the silicide electrical contact areas comprise a metal silicide selected from the group consisting of $TiSi_2$ and $CoSi_2$.

10. (original) The method of claim 8, wherein the CMOS transistor forms a portion of a circuit selected from the group consisting of logic circuitry, memory circuitry, analog circuitry, or combinations thereof.

11. (previously presented) The method of claim 1, wherein steps a) through e are repeated to form at least 3 metallization layers over a PMD layer.

12. (previously presented) The method of claim 1, wherein steps a) through e are repeated to form a multi-level semiconductor device consisting essentially of AlCu wiring.

13. (currently amended) A method of forming a multi-level semiconductor device wiring interconnect structure according to a low temperature process to improve

electrical properties including an electro-migration resistance and electrical resistance comprising the steps of:

a) forming a dielectric insulating layer over a conductive portion;

wherein the conductive portion comprises salicide electrical contact areas comprising a CMOS transistor portion;

b) forming a via opening in closed communication with the conductive portion;

c) forming a barrier layer to line the via opening;

d) forming a layer of AlCu at a temperature less than about 400 °C to fill the via opening to form an AlCu via including a portion of said AlCu layer overlying the ~~first~~ dielectric insulating layer;

e) forming an AlCu interconnect line from said portion of said AlCu layer over the AlCu via; and,

f) optionally forming a second barrier layer on the AlCu interconnect line.

14. (previously presented) The method of claim 13, wherein steps b through f are repeated in overlying dielectric insulating layers to sequentially form AlCu vias and AlCu interconnect lines through at least 3 metallization levels.

15. (previously presented) The method of claim 13, wherein the step of forming an AlCu layer is a carried out at pressures less than about 5 milliTorr.

16. (original) The method of claim 13, wherein the dielectric insulating layer consists essentially of fluorinated silicate glass (FSG).

17. (previously presented) The method of claim 13, wherein the via openings are formed with an aspect ratio greater than 1.5.

18. (original) The method of claim 13, wherein the barrier layers are selected from the group consisting of Ti/TiN, TiN, Ta, TaN, and combinations thereof.

19. cancelled

20. (previously presented) The method of claim 13, wherein the salicide electrical contact areas comprise a metal silicide selected from the group consisting of $TiSi_2$ and $CoSi_2$.

21. (previously presented) The method of claim 13, wherein the CMOS transistor forms a portion of a circuit selected from the group consisting of logic circuitry, memory circuitry, analog circuitry, and combinations thereof.

22. (currently amended) The method of claim 13, wherein steps b through f are repeated in overlying dielectric insulating layers to form at least 3 metallization layers over a PMD layer.

23. (previously presented) The method of claim 13, wherein steps b through f are repeated in overlying dielectric insulating layers to form a multi-level semiconductor device consisting essentially of AlCu wiring.

24. (previously presented) A multi-level wiring interconnect structure for a semiconductor device comprising:

a) a dielectric insulating layer over a conductive portion said conductive portion selected from the group consisting of tungsten, metal silicide, copper, and AlCu;

b) an AlCu via comprising a first barrier layer formed in the dielectric insulating layer in closed communication with the conductive portion;

c) an AlCu interconnect line disposed on and contiguous with the AlCu via;

wherein a second barrier layer encapsulates the AlCu interconnect line on three sides.

25. (original) The multi-level wiring interconnect structure of claim 24, wherein structure portions a) through c) are stacked sequentially to comprise at least three metallization layers.

26. cancelled

27. (original) The multi-level wiring interconnect structure of claim 24, wherein structure portions a) through c) are stacked sequentially to form a multi-level semiconductor device consisting essentially of AlCu wiring.

28. (original) The multi-level wiring interconnect structure of claim 24, wherein the dielectric insulating layer is selected from the group consisting of carbon doped silicon oxide, organo silicate glass (OSG), and fluorinated silicate glass (FSG).

29. (original) The multi-level wiring interconnect structure of claim 24, wherein the dielectric insulating layer consists essentially of fluorinated silicate glass (FSG).

30. (original) The multi-level wiring interconnect structure of claim 24, via openings are formed with an aspect ratio greater than 1.5.

31. (original) The multi-level wiring interconnect structure of claim 24, wherein the first and second barrier layers are selected from the group consisting of Ti/TiN, TiN, Ta, TaN, and combinations thereof.

32. (original) The multi-level wiring interconnect structure of claim 24, wherein the conductive portion comprises silicide electrical contact areas comprising a CMOS transistor portion selected from the group consisting of a gate electrode and source and drain regions.

33. (previously presented) The multi-level wiring interconnect structure of claim32, wherein the silicide electrical contact areas comprise a metal silicide selected from the group consisting of $TiSi_2$ and $CoSi_2$.

34. (previously presented) The multi-level wiring interconnect structure of claim 32, wherein the CMOS transistor forms a portion of a circuit selected from the group consisting of logic circuitry, memory circuitry, analog circuitry, and combinations thereof.

35. (previously presented) A multi-level wiring interconnect structure for a semiconductor device comprising:

a) a dielectric insulating layer over a conductive portion;

wherein the conductive portion comprises salicide electrical contact areas comprising a CMOS transistor portion;

b) an AlCu via comprising a barrier layer lining the AlCu via opening, said via opening formed in the dielectric insulating layer in closed communication with the conductive portion;

wherein structure portions b is stacked sequentially in overlying dielectric insulating layers to comprise at least three metallization layers.

36. cancelled.

37. (previously presented) The multi-level wiring interconnect structure of claim 35, wherein structure portion b stacked sequentially in overlying dielectric insulating layers to form a multi-level semiconductor device consisting essentially of AlCu wiring.

38. (original) The multi-level wiring interconnect structure of claim 35, wherein the dielectric insulating layer is selected from the group consisting of carbon doped silicon oxide, organo silicate glass (OSG), and fluorinated silicate glass (FSG).

39. (original) The multi-level wiring interconnect structure of claim 35, wherein the dielectric insulating layer consists essentially of fluorinated silicate glass (FSG).

40. (previously presented) The multi-level wiring interconnect structure of claim 35, wherein said via opening is formed with an aspect ratio grater than 1.5.

41. (previously presented) The multi-level wiring interconnect structure of claim 35, wherein the barrier layer is selected from the group consisting of Ti/TiN, TiN, Ta, TaN, and combinations thereof.

42. cancelled

43. (previously presented) The multi-level wiring interconnect structure of claim 35, wherein the silicide electrical contact areas comprise a metal silicide selected from the group consisting of $TiSi_2$ and $CoSi_2$.

44. (previously presented) The multi-level wiring interconnect structure of claim 35, wherein the CMOS transistor forms a portion of a circuit selected from the group consisting of logic circuitry, memory circuitry, analog circuitry, and combinations thereof.

45. (previously presented) The method of claim 1, wherein the second barrier layer is formed to encapsulate said AlCu interconnect line on three sides.

46. (previously presented) The method of claim 13, wherein the second barrier layer is formed to encapsulate said AlCu interconnect line on three sides.

47. (previously presented) The multi-level wiring interconnect structure of claim 35, further comprising an AlCu interconnect line disposed on the AlCu via.

48. (previously presented) The multi-level wiring interconnect structure of claim 47 further comprising a second barrier layer on the AlCu interconnect line.